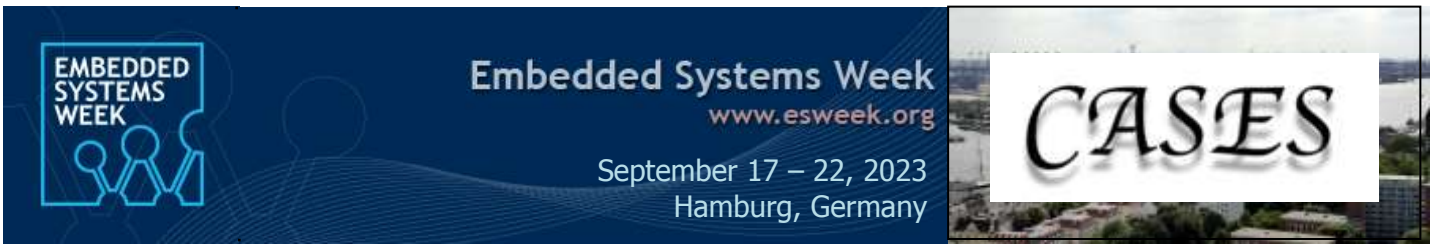

International Conference on Compilers, Architectures, and Synthesis for Embedded Systems
September 17 – September 22, 2023, *Hamburg, Germany*

CASES is a premier forum, where researchers, developers, and practitioners exchange information on the latest ad-vances in design, optimization, validation, and applications of embedded systems, Internet of Things (IoT), and the emergent trend of integrating Artificial Intelligence into IoT (AIoT). The conference has a long tradition of showcasing cutting-edge research in these broad areas, covering topics including, but not limited to, hardware-software co-design and co-validation, edge AI, embedded architecture, memory/storage technology, security/reliability, energy-efficiency of embedded systems, and domain-specific hardware accelerators.

LB/WiP Paper Submissions: May 22, 2023 (firm)
First round of notification: June 2, 2023
Submit revision: June 19, 2023
Final notification: July 3, 2023

Late-Breaking (LB) Result papers provide a venue for quick dissemination of research ideas to the embedded systems community and are expected to represent complete and mature works written in a condensed form.

Work-in-Progress (WIP) papers are intended as a venue to report early or ongoing research activities representing work that has not been fully realized or developed, for which full empirical data may not yet be available, or that has not yet reached a level of maturity expected for other types of submissions.

Submissions are invited on all aspects of embedded systems, including but not limited to:

- AI Systems and Applications of AI at Edge
  - Architectures, accelerators, and compilers for artificial intelligence hardware
  - Applications of machine learning techniques to embedded systems, IoT, and CPS
  - Neuromorphic and cognitive computing, analytics for embedded applications
- Embedded Systems and IoT/CPS Security
  - Secure architectures and hardware security
  - Software security for embedded systems, IoT, and CPS
- Memory and Storage
  - Memory system architecture
  - Emerging memory technologies
  - Caches, scratchpad memory, and compiler-controlled memory
  - Reconfigurable memory and storage systems
- Accelerators, Emerging Technologies, and Applications
  - Design space exploration of accelerators
  - Domain-specific accelerators for emerging applications including AI and graph analytics
  - Heterogeneous multi-core SoC
  - Biologically inspired computing and approximate computing
- Architectures, Compilers, System-level Design
  - Embedded and processor micro-architecture
  - Manycore architectures and Reconfigurable computing including FPGAs and CGRAs
  - Compiler support for CPU, GPU, and reconfigurable computing

ESWEEK invites you to submit original research articles for LB (up to 4 pages) and WIP (up to 2 pages) papers, in IEEE/ACM 10 pt double-column format. Both LB and WIP papers will go through 2 rounds of reviews. If accepted, LB papers will be published in IEEE Embedded Systems Letters, while WIP papers will be published in ESWEEK proceedings of the respective conferences. Authors of accepted LB and WIP papers will present a poster of their work, and a lightning talk at ESWEEK. Authors of accepted LB papers will also need to submit a 3-minute video with their final camera-ready version (to be uploaded to the submission system following instructions communicated in the acceptance notifications).

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