Call for Late-Breaking (LB) and Work-in-Progress (WIP) Papers

International Conference on Hardware/Software Codesign and System Synthesis

September 17 – September 22, 2023, *Hamburg, Germany*

The International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS) is the premier conference in system-level design, hardware/software co-design, modeling, analysis, and implementation of modern Embedded Systems, Cyber-Physical Systems, and Internet-of-Things, from system-level specification and optimization to synthesis of system-on-chip hardware/software implementations. CODES+ISSS is part of Embedded Systems Week (ESWEEK), the premier event covering all aspects of hardware and software design for smart, intelligent, and connected computing systems.

CODES+ISSS Program Chairs:
Mohammad Abdullah Al Faruque, University of California, Irvine, USA
Muhammad Shafique, New York University (NYU) Abu Dhabi, UAE

Timeline of LB/WIP Papers

LB/WIP Paper submission (firm): 22.May.2023

First round of notification: 02.June.2023

Submit revision: 19.June.2023

Final notification: 03.July.2023

Camera-ready submission: 13.July. 2023

Late-Breaking (LB) Result papers provide a venue for quick dissemination of research ideas to the embedded systems community and are expected to represent complete and mature works written in a condensed form.

Work-in-Progress (WIP) papers are intended as a venue to report early or ongoing research activities representing work that has not been fully realized or developed, for which full empirical data may not yet be available, or that has not yet reached a level of maturity expected for other types of submissions.

Topics of interest include:

Track 1) System-level design – Specification, modelling, refinement, synthesis, and partitioning of embedded systems, hardware-software co-design, hybrid system modeling and design, model-based design, design for adaptivity and reconfigurability.

Track 2) Domain and application-specific design – Analysis, design, and optimization techniques for multimedia, medical, automotive, cyber-physical, IoT, and other application domains.

Track 3) System architecture – Heterogeneous systems, many-cores, and distributed systems, architecture and micro-architecture design, exploration and optimizations of application-specific processors and accelerators, reconfigurable and self-adaptive architectures, storage, memory systems, and networks-on-chip.

Track 4) Simulation, validation, and verification – Hardware/software co-simulation, verification and validation methodologies, formal verification, hardware accelerated simulation, simulation and verification languages, models, and benchmarks.

Track 5) Embedded software – Language and library support, compilers, runtimes, parallelization, software verification, memory management, virtual machines, operating systems, real-time support, middleware.

Track 6) Safety, security, and reliability – Cross-layer reliability, resiliency and fault tolerance, test methodology, design for security, reliability, and testability, hardware security, security for embedded, CPS, and IoT devices.

Track 7) Power-aware systems – Power-aware and energy-aware system design and methodologies, ranging from low-power embedded and cyber-physical systems, IoT devices, to energy-efficient large-scale systems such as cloud datacenters, green computing, and smart grids.

Track 8) Embedded machine learning – Hardware and software design, implementation, and optimization for machine learning that are specially designed for resource- and power-constrained embedded, CPS, and IoT devices.

Track 9) Industrial practices and case studies – Practical impact on current and/or future industries, application of state-of-the-art methodologies and tools in areas including wireless, networking, multimedia, automotive, cyber-physical, medical systems, IoT, etc.

ESWEEK invites you to submit original research articles for LB (up to 4 pages) and WIP (up to 2 pages) papers, in IEEE/ACM 10 pt double-column format. Both LB and WIP papers will go through 2 rounds of reviews. If accepted, LB papers will be published in IEEE Embedded Systems Letters, while WIP papers will be published in ESWEEK proceedings of the respective conferences. Authors of accepted LB and WIP papers will present a poster of their work, and a lightning talk at ESWEEK. Authors of accepted LB papers will also need to submit a 3-minute video with their final camera-ready version (to be uploaded to the submission system following instructions communicated in the acceptance notifications).

ESWEEK General Chairs:
Xiaobo Sharon Hu, University of Notre Dame, USA
Alain Girault, INRIA, France

CODES+ISSS Program Chairs:
Mohammad Al Faruque, Univ. of California, Irvine, USA
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