CODES+ISSS 2020

Call for Papers

International Conference on Hardware/Software Codesign and System Synthesis
September 20 - 25, 2020, Virtual Conference

The International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS) is the premier conference in system-level design, hardware/software co-design, modeling, analysis, and implementation of modern embedded and cyber-physical systems, from system-level specification and optimization to system synthesis of multiprocessor hardware/software implementations. CODES+ISSS is part of Embedded Systems Week (ESWEEK), the premier event covering all aspects of hardware and software design for smart, intelligent and connected computing systems.

CODES+ISSS Program Chairs:
Roman Lysecky, University of Arizona, USA
Jason Xue, City University of Hong Kong, China

Journal Track Submissions:
Abstracts: April 03, 2020
Full Paper: ~~April 10, 2020~~
April 17, 2020 (extended, firm)

Work-in-Progress Submissions:
Paper submission: ~~June 05, 2020~~
June 12, 2020 (extended)

Notification of Acceptance:
July 06, 2020 (both tracks)

Topics of interest include:

Track 1) System-level design – Specification, modeling, refinement, system synthesis, partitioning, hardware-software co-design, design space exploration, hybrid system modeling and design, model-based design, and design for adaptivity and reconfigurability.

Track 2) Domain and application-specific design – Analysis, design, and optimization techniques for multimedia, medical, automotive, cyber-physical, Internet of Things (IoT), and other application domains.

Track 3) Embedded software – Language and library support, compilers, runtimes, parallelization, software verification, memory management, virtual machines, operating systems, real-time support, middleware.

Track 4) Safety, security and reliability – Cross-layer reliability, resilience and fault tolerance, test methodology, design for testability, hardware and software security, security for embedded and IoT devices, and cyber-physical system security.

Track 5) Simulation, validation and verification – Hardware/software co-simulation, verification and validation methodologies, formal verification, hardware accelerated simulation, simulation and verification languages, models, and benchmarks.

Track 6) System architecture – Heterogeneous systems, many-cores, networked and distributed systems, architecture and micro-architecture design, exploration and optimization including application-specific processors, reconfigurable and self-adaptive architectures, storage, memory systems, and networks-on-chip.

Track 7) Power-aware systems – Power-aware and energy-aware system design and methodologies ranging from low-power embedded and cyber-physical systems to energy-efficient large-scale systems such as cloud datacenters, green computing, and smart grids.

Track 8) Industrial practices and case studies – Practical impact on current and/or future industries, application of state-of-the-art methodologies and tools in various application areas including wireless, networking, multimedia, automotive, cyber-physical, medical systems, IoT, etc.

A Special Day on Trustworthy IoT will be organized jointly by all conferences in ESWEEK.

Journal-integrated Publication Model: Journal-integrated Publication Model: All accepted full papers will be published in the IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD).

ESWEEK General Chairs:
Tulika Mitra, National University of Singapore, SG
Andreas Gerstlauer, University of Texas at Austin, USA

CODES+ISSS Program Chairs:
Roman Lysecky, University of Arizona, USA
Jason Xue, City University of Hong Kong, China

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